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**1** [Geometric programming: a programming approach to geometric design](#)

97%

Alberto Paoluzzi , Valerio Pascucci , Michele Vicentino

ACM Transactions on Graphics (TOG) July 1995

Volume 14 Issue 3

This article presents a functional programming approach to geometric design with embedded polyhedral complexes. Its main goals are to show the expressive power of the language as well as its usefulness for geometric design. The language, named PLASM (the Programming Language for Solid Modeling), introduces a very high level approach to “constructive” or “generative” modeling. Geometrical objects are generated by evaluating some suitable language expressions. Because ...

2 [Gate sizing with controlled displacement](#)

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Wei Chen , Cheng-Ta Hsieh , Massoud Pedram

Proceedings of the 1999 international symposium on Physical design April 1999**3** [Concurrent logic restructuring and placement for timing closure](#)

88%

Jinan Lou , Wei Chen , Massoud Pedram

Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design November 1999


In this paper, an algorithm for simultaneous logic restructuring and placement is presented. This algorithm first constructs a set of super-cells along the critical paths and then generates the set of non-inferior re-mapping solutions for each supercell. The best mapping and placement solutions for all super-cells are obtained by solving a generalized geometric programming (GGP) problem. The process of identifying and optimizing the critical paths is iterated until timing closure is achieved ...

- 4 Model order reduction: Realizable parasitic reduction using generalized Y- π transformation 87%
 4 Zhanhai Qin , Chung-Kuan Cheng
Proceedings of the 40th conference on Design automation June 2003
 We propose a realizable RCLK-in-RCLK-out parasitic reduction technique. The method employs generalized Y- π transformation. In our method, admittances are kept in their original rational forms of s, and their orders are reduced by truncating high-order terms. Therefore reduced admittances match the low-order terms in exact admittances. First-order realization of admittances is guaranteed, and higher-order realization is achieved by template optimization using Geometric Programming. The algor ...
- 5 On translating geometric solids to functional expressions 82%
 4 Omid Banyasad , Philip T. Cox
Proceedings of the 5th ACM SIGPLAN international conference on Principles and practice of declarative programming August 2003
 Language for Structured Design (LSD) is a high level, visual, logic programming language for design of structured objects. LSD combines the design and programming activities in a homogeneous programming/design environment by extending Lograph, a visual logic programming language, with the notion of solids and operations on them. At the back-end, however, a solid modeling kernel for maintaining low level description of solids and operations is required. In this paper, we report on our progress towa ...
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 In this paper we present a method for the design of analog-to-digital converters (ADCs). This method computes the sizes of the different components (transistors, capacitors, etc.) in a predefined ADC topology so that the design specifications are met in the desired process technology. The method is based on formulating the ADC design constraints such as specifications on power, signal-to-noise ratio (SNR), area, and sampling frequency in special convex form in terms of the component sizes of the A ...
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 We present a method for optimizing and automating component and transistor sizing for CMOS LC oscillators. We observe that the performance measures can be formulated as posynomial functions of the design variables. As a result, the LC oscillator design problems can be posed as a geometric program, a special type of optimization problem for which very efficient global optimization methods have recently been developed. The synthesis method is ...
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Proceedings of the fourth annual conference on Applications of simulation December 1970
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 K. S. Trivedi
Proceedings of the 7th annual symposium on Computer Architecture May 1980
 A geometric programming model is proposed to determine the optimal design of the CPU and its matching storage hierarchy. The objective function is the maximization of system reliability subject to performance and budgetary limitations. Examples illustrating the use of the model are presented.
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 In this paper we present a method for determining the feasible set of analog design problems and we propose an efficient method for their verification. The verification method presented relies on the formulation of the analog circuit design problem as a convex optimization problem in both the design variables and the performance specifications. Since the design is convex not only in the design variables but also in the specification parameters, we observe that the feasible sets are convex and po ...
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 Hua Tang , Hui Zhang , Alex Doboli
Proceedings of the 13th ACM Great Lakes Symposium on VLSI April 2003
 This paper describes a layout-aware analog synthesis methodology. The methodology includes parameter exploration and classification, parameter domain pruning and sampling, and identification of parameter dependencies. The optimization process executes a combined constraint transformation, floorplanning and global routing. The paper presents results for a high frequency continuous-time filter, and two ?? ADCs. Compared to similar work, the methodology is more flexible in handling new de ...
- 14 Analog synthesis & design methodology: An efficient optimization--based technique to generate posynomial performance models for analog integrated circuits 80%
 Walter Daems , Georges Gielen , Willy Sansen
Proceedings of the 39th conference on Design automation June 2002
 This paper presents an new direct--fitting method to generate posynomial response surface

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15 Closed form solutions to simultaneous buffer insertion/sizing and wire sizing 80%

 Chris Chu , D. F. Wong

ACM Transactions on Design Automation of Electronic Systems (TODAES) July 2001
Volume 6 Issue 3

In this paper, we consider the delay minimization problem of an interconnect wire by simultaneously considering buffer insertion, buffer sizing and wire sizing. We consider three cases, namely using no buffer (i.e., wire sizing alone), using a given number of buffers, and using the optimal number of buffers. We provide elegant closed form optimal solutions for all three problems. These closed form solutions are useful in early stages of the VLSI design flow such as logic synthesis and floo ...


16 A polynomial time optimal algorithm for simultaneous buffer and wire sizing 80%

 C. C. N. Chu , D. F. Wong

Proceedings of the conference on Design, automation and test in Europe February 1998

An interconnect joining a source and a sink is divided into fixed-length uniform-width wire segments, and some adjacent segments have buffers in between. The problem we considered is to simultaneously size the buffers and the segments so that the Elmore delay from the source to the sink is minimized. Previously, no polynomial time algorithm for the problem has been reported in literature. In this paper, we present a polynomial time algorithm \mathit{SBWS} for the simultaneous buffer and wire si ...

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 Gabriel M. Silberman


Communications of the ACM November 1983
Volume 26 Issue 11

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 J. J. Dinkel , Mary S. Kochenberger , S. N. Wong

ACM Transactions on Mathematical Software (TOMS) March 1978
Volume 4 Issue 1

19 CYCLONE: automated design and layout of RF LC-oscillators 80%


 C. De Ranter , B. De Muer , G. Van der Plas , P. Vancorenland , M. Steyaert , G. Gielen , W. Sansen

Proceedings of the 37th conference on Design automation June 2000



This paper presents an automated, layout-aware RF LC-oscillator design tool, called CYCLONE that delivers an accurate and optimal LC-oscillator design, from specification to layout. The tool combines the accuracy of device-level simulation and finite element analysis with the optimisation power of simulated annealing algorithms and is verified with experimental results.

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80%

 Kishor S. Trivedi , Timothy M. Sigmon
Journal of the ACM (JACM) April 1981
Volume 28 Issue 2

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Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design
November 1999

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ACM Transactions on Mathematical Software (TOMS) March 1978
Volume 4 Issue 15 [Design of pipeline analog-to-digital converters via geometric programming](#) 83%

Maria del Mar Hershenson


Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design

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6 Concurrent logic restructuring and placement for timing closure

83%

 Jinan Lou , Wei Chen , Massoud Pedram

Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design
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7 Macro-driven circuit design methodology for high-performance datapaths

77%


 Mahadevamurty Nemani , Vivek Tiwari

Proceedings of the 37th conference on Design automation June 2000

Datapath design is one of the most critical elements in the design of a high performance microprocessor. However datapath design is typically done manually, and is often custom style. This adversely impacts the overall productivity of the design team, as well as the quality of the design. In spite of this, very little automation has been available to the designers of high performance datapaths. In this paper we present a new "macro-driven" approach to the design of datapath circuits ...

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